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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,370	04/23/2001	Masaru Iida	010570	2325

38834 7590 01/12/2006

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
PHAM, HAI CHI	

ART UNIT	PAPER NUMBER
2861	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,370	IIDA, MASARU	
	Examiner	Art Unit	
	Hai C. Pham	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed 11/16/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7 and 8* is/are rejected.

7)☒ Claim(s) *2-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/16/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request For Continued Examination

1. The request filed on 11/16/05 for a Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/839,370 is acceptable and a RCE has been established. An action on the RCE follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Utsugi (JP 2-67665) in view of Maas et al. (U.S. 6,763,036).

Utsugi, an acknowledged prior art, discloses a data sequence conversion circuit, which takes as an input any one of a plurality of input data sequences having different data widths (e.g., 8-bit or 16-bit data), and which converts said input data sequence into an output data sequence having a prescribed data width (e.g., 16-bit data) for output, said circuit comprising a first parallel shift register (register 31) for holding said input data sequence, and a second parallel shift register (registers 32, 33) for outputting said input data as a data sequence having said prescribed data width (16-bit data) (see Abstract).

Although Utsugi is silent with regard to the switch matrix for taking the data held in said first parallel shift register as input data, and for outputting said input data in a distributed fashion to said second parallel shift register, a certain logic circuit or switch matrix is necessary included so as to control the flow of data between the two registers. However, Utsugi fails to teach such logic circuit or switch matrix outputting said input data in a distributed fashion to said second parallel shift register in accordance with a rule selected by a control signal from a plurality of predetermined rules.

Maas et al. discloses in Fig. 1 an apparatus comprising a first serial-to-parallel register (register section 102 comprising the serial-to-parallel register 108 and two parallel registers 110 and 112) for receiving an input data (SERIAL IN 116), second parallel registers (multiplexer 106) for outputting an output signal (OUTPUT 146) according to the logic circuit (symbol detector 104), which receives a programmable signal (framing symbol signal FS) so as to determine the framed output (146) for the input signal (116).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the logic circuit in the device of Utsugi as taught by Maas et al. for the purpose of controlling the conversion of the data so as to obtain the output signal with a selected bit width.

With regard to claim 7, Utsugi further teaches each time QIn data sequences (e.g., two consecutive sequences) are input into said first parallel shift register (31), Wn.times.QIn units of data (e.g., 8 x 2 bits) are input into said second parallel shift

registers (32 and 33), following which QOn data sequences are output from said second parallel shift register (e.g., sequences of 16-bit data being outputted).

4. Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Acknowledged Prior Art (hereinafter referred as AAPA) in view of Utsugi and Maas et al.

AAPA discloses an LED printer comprising a data sequence conversion circuit (60) located between a jaggy correction circuit (50) and a line printhead (26) (Fig. 7).

However, AAPA fails to teach the first parallel shift register, the switch matrix and the second parallel shift register.

Utsugi, an acknowledged prior art, discloses a data sequence conversion circuit, which takes as an input any one of a plurality of input data sequences having different data widths (e.g., 8-bit or 16-bit data), and which converts said input data sequence into an output data sequence having a prescribed data width (e.g., 16-bit data) for output, said circuit comprising a first parallel shift register (register 31) for holding said input data sequence, and a second parallel shift register (registers 32, 33) for outputting said input data as a data sequence having said prescribed data width (16-bit data) (see Abstract).

On the other hand, Maas et al. discloses in Fig. 1 an apparatus comprising a first serial-to-parallel register (register section 102 comprising the serial-to-parallel register 108 and two parallel registers 110 and 112) for receiving an input data (SERIAL IN 116), second parallel registers (multiplexer 106) for outputting an output signal

(OUTPUT 146) according to the logic circuit (symbol detector 104), which receives a programmable signal (framing symbol signal FS) so as to determine the framed output (146) for the input signal (116).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide AAPA device with the first parallel shift register, the switch matrix and the second parallel shift register as taught by Utsugi and Maas et al. The motivation for doing so would have been to adapt the printer to receive the input data with different bit widths and to output a driving signal of selected bit width to drive the LEDs of the printhead.

Allowable Subject Matter

5. Claims 2-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The reason for the allowability of claims 2-6 has been indicated in the previous Office action issued on 02/24/05.

Pertinent Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Long et al. (U.S. 4,984,249) discloses a data sequence conversion circuit including a first parallel register, a decision logic circuit and an output latch circuit.

Hirata et al. (U.S. 6,891,424) discloses a data sequence conversion circuit including a first parallel register, a switch matrix circuit and an output multiplexer circuit.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai C. Pham whose telephone number is (571) 272-2260. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (571) 272-1934. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hai C. Pham

HAI PHAM
PRIMARY EXAMINER

January 5, 2006